AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (*Currently Amended*) A delay analysis system for making a delay analysis of a logic circuit,

said system having a delay analysis library comprising connection information and delay time information for a plurality of circuits,

wherein, for at least one of said plurality of circuits, said library further comprises logical operation information representing correspondence between logical state transitions at each input terminal of said at least one circuit and logical state transitions at each output terminal of said at least one circuit, and said delay information for said at least one circuit is based upon ~~a~~ logical state transitions ~~transition~~ at said ~~an~~ input terminals ~~terminal~~ and ~~its~~ corresponding logical state transitions ~~transition~~ at said ~~an~~ output terminals ~~terminal~~ as represented by said logical operation information for said at least one circuit, and

when making a delay analysis of each path of the logic circuit comprising said at least one circuit, a delay time is selected from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on the last input terminal to transition from a low state to a high state that causes said selected output terminal to transition from a low state to a high state according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, said delay

time is selected based on the first input terminal to transition from a high state to a low state that causes said selected output terminal to transition from a high state to a low state according to the logical operation information ~~according to the type of logical state transitions present at selected input and output terminals of said at least one circuit~~.

2. (*Currently Amended*) A delay analysis system for making a delay analysis of a logic circuit, said system having a delay analysis library comprising connection information and delay time information for a plurality of circuits,

wherein, for at least one of said plurality of circuits, said library further comprises logical operation information representing correspondence between logical state transitions at each input terminal of said at least one circuit and logical state transitions at each output terminal of said at least one circuit, and said delay information for said at least one circuit is based upon ~~a~~ logical state transitions ~~transition~~ at said ~~an~~ input terminals ~~terminal~~ and ~~its~~ corresponding logical state transitions ~~transition~~ at said ~~an~~ output terminals ~~terminal~~ as represented by said logical operation information for said at least one circuit, and

when making a delay analysis of a logic circuit, a delay time of each path between a plurality of ~~selected~~ input terminals ~~terminal~~ and a selected output terminal of said at least one circuit is selected from said delay time information, wherein if said selected output terminal transitions from a low state to a high state, said delay time is selected based on the last input terminal of said plurality of input terminals to transition from a low state to a high state that causes said selected output terminal to transition from a low state to a high state according to the

logical operation information, or if said selected output terminal transitions from a high state to a low state, said delay time is selected based on the first input terminal of said plurality of input terminals to transition from a high state to a low state that causes said selected output terminal to transition from a high state to a low state according to the logical operation information ~~according to the type of logical state transitions present at said selected input and output terminals of said at least one circuit~~.

3. (*Currently Amended*) A method for making a delay analysis of a logic circuit, comprising the steps of:

referencing a delay analysis library for a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information representing correspondence between logical state transitions at each input terminal and logical state transitions at each output terminal of at least one of said plurality of circuits, said delay information for said at least one circuit is based upon ~~a~~ logical state transitions ~~transition~~ at said ~~an~~ input terminals ~~terminal~~ and ~~its~~ corresponding logical state transitions ~~transition~~ at said ~~an~~ output terminals ~~terminal~~ as represented by said logical operation information for said at least one circuit; and

if the logic circuit comprises said at least one circuit, selecting the delay time of each path of said at least one circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on the last input terminal to transition from a low state to a high state that causes said selected output terminal to

transition from a low state to a high state according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, said delay time is selected based on the first input terminal to transition from a high state to a low state that causes said selected output terminal to transition from a high state to a low state according to the logical operation information~~according to the type of logical state transitions present at selected input and output terminals of said at least one circuit~~.

4. (*Currently Amended*) A computer-readable medium having stored thereon a program for executing:

a process step comprising:

referencing a delay analysis library for a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information representing correspondence between logical state transitions at each input terminal and logical state transitions at each output terminal of each one of said plurality of circuits, said delay information for said at least one circuit is based upon ~~a~~ logical state transitions ~~transition~~ at said ~~an~~ input terminals ~~terminal~~ and ~~its~~ corresponding logical state transitions ~~transition~~ at said ~~an~~ output terminals ~~terminal~~ as represented by said logical operation information for said at least one circuit; and

if a logic circuit comprises said at least one circuit, selecting the delay time of each path of said at least one circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on

the last input terminal to transition from a low state to a high state that causes said selected output terminal to transition from a low state to a high state according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, said delay time is selected based on the first input terminal to transition from a high state to a low state that causes said selected output terminal to transition from a high state to a low state according to the logical operation information~~according to the type of logical state transitions present at selected input and output terminals of said at least one circuit~~; and

a process step of performing a delay calculation using said selected delay time as a propagation delay time of said at least one circuit.